IN THE CLAIMS

1. (Original) A NAND-type flash memory device including a memory cell array having a plurality of memory blocks, comprising:

a status cell array having a plurality of status cells and structured to store data indicating an erase/program status of the memory blocks;

a data generation circuit structured to generate data indicating a program status of a selected memory block in response to a data input command and to generate data indicating an erase status of a selected memory block in response to a block erase setup command;

a first signal generation circuit structured to generate a block status write enable signal and a clock signal in response to either one of an erase command and a program command;

a selection circuit structured to select at least one of the status cells of the status cell array in response to a block address of the selected memory block;

a write circuit which is structured to receive data from the data generation circuit in response to the clock signal during a program or erase operation and to write the received data in the selected status cell; and

a control circuit structured to operate in response to a block status write enable signal from the first signal generation circuit and to control the write circuit to the store the data inputted to the write circuit in a selected status cell when an erase/program operation for the selected memory block is carried out.

2. (Original) The NAND-type flash memory device of claim 1, wherein the status cells are overwritable non-volatile memory cells.

3. (Original) The NAND-type flash memory device of claim 1, wherein the first signal generation circuit includes:

a first signal generator for generating a first block write enable signal and a first clock signal in response to the erase command; and

a second signal generator for generating a second block status write enable signal and a second clock signal in response to the program command.

4. (Original) The NAND-type flash memory device of claim 3, wherein the first signal generator includes:

a decoder for decoding the erase command to generate a block status write flag signal;

a latch for latching the block status write flag signal from the decoder in response to a write enable signal; and

a clock generator for generating the first clock signal in response to an output signal of the latch.

5. (Original) The NAND-type flash memory device of claim 3, wherein the second signal generator includes:

a decoder for decoding the program command to generate a block status write flag signal;

a latch for latching the block status write flag signal from the decoder in response to a write enable signal; and

a clock generator for generating the second clock signal in response to an output signal of the latch.

6. (Original) The NAND-type flash memory device of claim 1, further comprising:

a second signal generation circuit structured to generate a block status read enable signal in response to a block status write command for writing data of the status cells; and

a read circuit structured to read data from a status cell corresponding to a block address to be erased/programmed.

7. (Original) The NAND-type flash memory device of claim 6, wherein the control circuit is structured to control the read circuit in response to the block status read enable signal, and the data read by the read circuit is outputted to the outside through an output circuit.

8. (Original) A NAND-type flash memory device including a memory cell array having a plurality of memory blocks, comprising:

a status cell array having a plurality of status cells and structured to store data indicating an erase/program status of the memory blocks;

a write circuit for storing data into the status cell array when a state of one or more of the plurality of memory blocks changes; and

a read circuit for reading data from the status cell array.

9. (Original) The memory device of claim 8 wherein the status cell array can be read faster than one of the memory blocks can be read.

10. (Original) The memory device of claim 8, further comprising:

a data generation circuit structured to generate data indicating a program status of a selected memory block in response to a data input command and to generate data indicating an erase status of a selected memory block in response to a block erase command.

11. (Original) The memory device of claim 8, further comprising:

a first signal generation circuit structured to generate a block status write enable signal and a clock signal in response to either one of an erase command and a program command.

12. (Original) The memory device of claim 8, further comprising:

a selection circuit structured to select at least one of the status cells of the status cell array in response to a block address of the selected memory block.

13. (Original) A method of operating a memory device, comprising:

receiving a command to program a selected block of memory cells;

reading a cell in a status cell array located within the memory device that indicates a program/erase status of the selected block; and

programming the selected block when the cell in the status array indicates the selected block is in an erased state.

14. (Original) The method of claim 13, further comprising:

reading another cell in the status cell array when the cell in the status array indicates the selected block is in a programmed state.

15. (Original) The method of claim 13, further comprising:

writing to the status cell array data indicating an erased state after receiving a command to erase a selected block of memory cells.

16. (Original) The method of claim 15, wherein writing to the status cell array comprises writing data to overwriteable memory cells.

17. (Original) The method of claim 13, wherein reading data from the cell status array is faster than reading data from the selected block of memory cells.